What is claimed is:

1. A semiconductor device comprising

a lead frame having inner connecting portions and outer connecting portions,

a semiconductor chip having electrodes on a surface thereof,

metal wires for electrically connecting the electrodes on the semiconductor chip and the inner connecting portions of the lead frame,

a sealing resin for sealing the inner connecting portions of the lead frame, the semiconductor chip and the metal wires therein, and at the same time exposing the outer connecting portions of the lead frame at a bottom surface thereof, and

an inner connecting portion sealing resin for covering the inner connecting portion at the bottom side of the sealing resin.

2. A semiconductor device as claimed in claim 1, in which

each of the metal wires is bonded to an upper surface of the inner connecting portion;

a lower surface of the inner connecting portion is offset inwardly of the sealing resin with respect to the bottom surface of the sealing resin; and

a part of the sealing resin enters an underside of the inner connecting portion to form the inner connecting portion sealing resin.

3. A semiconductor device as claimed in claim 2, in which a step is formed between a lower surface of the outer connecting portion and the lower surface of the inner connecting portion.

4. A semiconductor device as claimed in claim 2, in which a tapered surface, which comes upwardly as it comes inwardly of the sealing resin, is provided between a

lower surface of the outer connecting portion and the lower surface the inner connecting portion.

5. A semiconductor device as claimed in claim 1, in which a head end of the outer connecting portion is substantially in a same plane with a side surface of the sealing resin.

6. A semiconductor device as claimed in claim 1, in which a bottom surface of the outer connecting portion is exposed from the bottom surface of the sealing resin to form an outer lead potion.

7. A semiconductor device as claimed in claim 1, in which a lead terminal portion including the inner connecting portion and the outer connecting portion has a wide portion and a narrow portion at shifted positions in the longitudinal direction thereof.

8. A semiconductor device as claimed in claim 1, in which at least a part of a section of a lead terminal portion including the inner connecting portion and the outer connecting portion is in a shape of an inverted trapezoid.

9. A lead frame comprising

a supporting portion for supporting a semiconductor chip, and

lead terminal portions each having an inner connecting portion to be electrically connected to the semiconductor chip to be mounted on the supporting portion and an outer connecting portion for outer connection,

a lower surface of the inner connecting portion being offset with respect to a lower surface of the outer connecting portion so that an inner connecting portion sealing space is defined below the inner connecting portion.

10. A lead frame as claimed in claim 9, in which a step is formed between the lower surface of the outer connecting portion and the lower surface of the inner connecting portion.

11. A lead frame as claimed in claim 9, in which a tapered surface, which comes upwardly as it comes toward the supporting portion, is provided on the lower surface of the inner connecting portion.

12. A lead frame as claimed in claim 9, in which the lead terminal portion has a wide portion and a narrow portion at shifted positions in a longitudinal direction thereof.

13. A lead frame as claimed in claim 9, in which at least a part of a section of the lead terminal portion is in a shape of an inverted trapezoid.